REMARKS

The Office Action refers to claims as being anticipated under 35 U.S.C. 102(e) by Takahashi, *et al.* (United States Patent Number 6,084,386), but does not explicitly state which claims are anticipated under 35 U.S.C. 102(e) based on Takahashi, *et al.* However, since the Office Action at pages 2-4 provides reasons as to why Takahashi, *et al.* discloses the limitations of claims 1, 3, 9, 30-32, 34, 35, 37, and 39-44, the remarks made herein are based on Applicants' belief that the Examiner intended to reject claims 1, 3, 9, 30-32, 34, 35, 37, and 39-44 as being anticipated under 35 U.S.C. 102(e) based on Takahashi, *et al.* Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi, *et al.* in view of Sher (United States Patent Number 6,633,196). Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi, *et al.* in view of Bae, *et al.* (United States Patent Number 6,373,754). Claims 33, 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi, *et al.* in view of Park, *et al.* (United States Patent Number 5,349,559). Claims 10-12, 14-17, 23, 25, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (United States Publication Number 2002/0053943) in view of Sher. In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references. Accordingly, reconsideration of the rejections is respectfully requested.

Independent claims 1 and 35 are amended herein to clarify that an internal voltage generating circuit of a semiconductor device comprises a comparing circuit comprising a switching circuit connected between an external power voltage and a first node, the switching circuit receiving a control signal and cutting off the external power voltage applied to a comparator of the comparing circuit when the control signal is activated. In addition, Independent claim 1 is amended herein to clarify that the internal voltage generating circuit comprises a driving signal control circuit receiving the control signal and inactivating a driving signal when the control signal is activated.

Independent claim 33 and 36 are amended herein to clarify that an internal voltage generating circuit of a semiconductor device comprises a comparing circuit comprising a first switching circuit connected between an external power voltage and a first node and cutting off the external power voltage applied to a comparator of the comparing circuit when a control signal is activated and a second switching circuit connected between a second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, wherein at least one of the first and second switching circuits receives the control signal. In addition, independent claims 33 and 36 are amended herein to clarify that the internal voltage generating circuit comprises a driving signal control circuit receiving the control signal and inactivating a driving signal when the control signal is activated.

Independent claims 34 and 37 are amended herein to clarify that an internal voltage generating circuit of a semiconductor device comprises a comparing circuit comprising a switching circuit connected between a first node and a ground voltage, the switching circuit receiving a control signal and cutting off a ground voltage supplied to a comparator of the comparing circuit when the control signal is activated. In addition, independent claims 34 and 37 are amended herein to clarify that the internal voltage generating circuit comprises a driving signal control circuit receiving the control signal and inactivating a driving signal when the control signal is activated.

Independent claim 38 is amended herein to clarify that an internal voltage generating circuit of a semiconductor device comprises a switching circuit receiving a control signal and transmitting a comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated. In addition, claim 38 is amended herein to clarify that a driving signal control circuit receives the control signal and inactivates a driving signal when the control signal is activated.

With regard to the rejections of independent claims 1 and 35 under 35 U.S.C. 102(e)

based on Takahashi, *et al.*, it is submitted that Takahashi, *et al.* fails to teach or suggest a semiconductor device comprising a semiconductor device that comprises an internal voltage generating circuit comprising a comparing circuit that, in turn, comprises a switching circuit connected between an external power voltage and a first node, the switching circuit receiving a control signal and cutting off the external power voltage applied to a comparator of the comparing circuit when the control signal is activated, as claimed in amended independent claims 1 and 35.

The Office Action at page 3 refers to a transistor QN1 of Takahashi, *et al.* as being a switching circuit. However, there is no teaching or suggestion in Takahashi, *et al.* of transistor QN1 being a switching circuit connected between an external power voltage and a first node, as claimed in amended independent claims 1 and 35. Instead, transistor QN1 of Takahashi, *et al.* is connected between a voltage comparing circuit 20 and a ground line 13 (see Takahashi, *et al.*, Figure 10).

Further, there is no teaching or suggestion in Takahashi, *et al.* of transistor QN1 being a switching circuit that receives a control signal, as claimed in claims 1 and 35. Instead, in Takahashi, *et al.*, transistor QN1 receives a control signal RAS (see Takahashi, *et al.*, Figure 10). Although the Office Action refers to an output /MD of a NAND gate 146 being a control signal generating circuit as being a control signal, there is no teaching or suggestion in Takahashi, *et al.* of the transistor QN1 receiving the output /MD of NAND gate 146.

In addition, it is submitted that Takahashi, *et al.* fails to teach or suggest a semiconductor device comprising a control signal generating circuit that receives an input signal and generates a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input

to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 1 and 35.

The Office Action repeatedly refers to refers to a load activation timing signal ACT of Takahashi, *et al.* as being an input signal. However, there is no teaching or suggestion in Takahashi, *et al.* of the load activation timing signal ACT being an input signal that is provided to a control signal generating circuit, and that is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34. Further, there is no no teaching or suggestion in Takahashi, *et al.* of a control signal being activated when the load activation timing signal ACT indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the load activation timing signal ACT indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 1 and 35. Further, there is no explanation in the Office Action as to the /MD signal of Takahashi, *et al.* being activated when ACT signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 1 and 35.

With regard to the rejection of independent claims 34 and 37 under 35 U.S.C. 102(e)

based on Takahashi, *et al.*, it is submitted that Takahashi, *et al.* fails to teach or suggest a semiconductor device comprising an internal voltage generating circuit comprising a comparing circuit that, in turn, comprises a switching circuit connected between a first node and a ground voltage, the switching circuit receiving a control signal and cutting off a ground voltage supplied to a comparator of the comparing circuit when the control signal is activated, as claimed in amended independent claims 34 and 37, for at least reasons similar to those described above with regard to claims 1 and 35. In addition, it is submitted that Takahashi, *et al.* fails to teach or suggest a control signal generating circuit receiving an input signal and generating a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 34 and 37, for at least reasons similar to those described above with regard to claims 1 and 35.

For at least the reasons described herein, it is submitted that Takahashi, *et al.* fails to teach or suggest the invention set forth in amended independent claims 1, 34, 35, and 37. Reconsideration and removal of the rejections of independent claims 1, 34, 35, and 37, and claims 3, 9, 30-32, and 39-44 dependent thereon under 35 U.S.C. 102(e) based on Takahashi, *et al.* are respectfully requested.

With regard to the rejections of claims 7 and 8 under 35 U.S.C. 103(a) based on the combination of Takahashi, *et al.* and Sher, Sher teaches a bond pad 20 connected to a plurality of

programmable circuits 16, 18, each comprising programmable fuses (see Sher, Figure 2, 2A and Abstract). However, it is submitted that Sher, like Takahashi, *et al.*, fails to teach or suggest a semiconductor device comprising a semiconductor device that comprises an internal voltage generating circuit comprising a comparing circuit that, in turn, comprises a switching circuit connected between an external power voltage and a first node, the switching circuit receiving a control signal and cutting off the external power voltage applied to a comparator of the comparing circuit when the control signal is activated, as claimed in amended independent claim 1. Further, it is submitted that Sher, like Takahashi, *et al.*, fails to teach or suggest a control signal generating circuit that receives an input signal and generates a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claim 1.

It is therefore submitted that neither Takahashi, *et al.* nor Sher teaches or suggests elements of the claims set forth above. Since neither Takahashi, *et al.* nor Sher teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Takahashi, *et al.* and Sher, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claims 7 and 8 are believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of claims 7 and 8 under

35 U.S.C. 103(a) based on the combination of Takahashi, *et al.* and Sher is respectfully requested.

With regard to the rejections of claim 2 under 35 U.S.C. 103(a) based on the combination of Takahashi, *et al.* and Bae, *et al.*, Bae, *et al.* teaches a semiconductor memory device including a memory cell array block 301 and a differential amplifier 303 that uses a reference voltage and an internal supply voltage fed back from the memory cell array block 301 as inputs, an internal supply voltage driver 305, pull down means 307, and control signal generating means 309 for generating a control signal CNT in response to an input signal PS (see Bae, *et al.*, Figure 3 and Abstract). However, it is submitted that Bae, *et al.*, like Takahashi, *et al.*, fails to teach or suggest a semiconductor device that comprises an internal voltage generating circuit comprising a comparing circuit that, in turn, comprises a switching circuit connected between an external power voltage and a first node, the switching circuit receiving a control signal and cutting off the external power voltage applied to a comparator of the comparing circuit when the control signal is activated, as claimed in amended independent claim 1. Further, it is submitted that Bae, *et al.*, like Takahashi, *et al.*, fails to teach or suggest a control signal generating circuit that receives an input signal and generates a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claim 1.

It is therefore submitted that neither Takahashi, *et al.* nor Bae, *et al.* teaches or suggests

elements of the claims set forth above. Since neither Takahashi, *et al.* nor Bae, *et al.* teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Takahashi, *et al.* and Bae, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claim 2 is believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of claim 2 under 35 U.S.C. 103(a) based on the combination of Takahashi, *et al.* and Bae, *et al.* is respectfully requested.

With regard to the rejections of independent claims 33, 36, and 38 under 35 U.S.C. 103(a) based on the combination of Takahashi, *et al.* and Park, *et al.,* it is submitted that Takahashi, *et al.* and Park, *et al.,* alone or in combination, fail to teach or suggest an internal voltage generating circuit of a semiconductor device comprises a comparing circuit comprising a first switching circuit connected between an external power voltage and a first node and cutting off the external power voltage applied to a comparator of the comparing circuit when a control signal is activated and a second switching circuit connected between a second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, wherein at least one of the first and second switching circuits receive the control signal, as claimed in amended independent claims 33 and 36, or an internal voltage generating circuit of a semiconductor device comprising a switching circuit receiving a control signal and transmitting a comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated, as claimed in amended independent claim 38.

Takahashi, *et al.* fails to teach or suggest an internal voltage generating circuit of a

semiconductor device comprising a comparing circuit comprising a first switching circuit connected between an external power voltage and a first node and cutting off the external power voltage applied to a comparator of the comparing circuit when a control signal is activated and a second switching circuit connected between a second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, wherein at least one of the first and second switching circuits receive the control signal, as claimed in amended independent claims 33 and 36, or an internal voltage generating circuit of a semiconductor device comprising a switching circuit receiving a control signal and transmitting a comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated, as claimed in amended independent claim 38, for at least reasons similar to those described above with regard to claims 1, 34, and 35.

Park, *et al.* teaches a circuit for generating an internal voltage to be supplied to memory elements during normal operation and providing an external voltage to the memory elements during a burn-in test operation (see Park, *et al.* Abstract). However, it is submitted that Park, *et al.*, like Takahashi, *et al.*, fails to teach or suggest an internal voltage generating circuit of a semiconductor device comprising a comparing circuit comprising a first switching circuit connected between an external power voltage and a first node and cutting off the external power voltage applied to a comparator of the comparing circuit when a control signal is activated and a second switching circuit connected between a second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, wherein at least one of the first and second switching circuits receive the control signal, as claimed in amended independent claims 33 and 36, or an internal voltage generating circuit of a semiconductor device comprising a switching circuit receiving a control signal and transmitting a comparing signal as a driving signal when the control signal is inactivated, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated, as claimed in amended independent claim 38.

In addition, it is submitted that Takahashi, *et al.* and Park, *et al.,* alone or in combination, fail to teach or suggest a control signal generating circuit receiving an input signal and generating a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 33, 36, and 38.

It is therefore submitted that neither Takahashi, *et al.* nor Park, *et al.* teaches or suggests elements of the claims set forth above. Since neither Takahashi, *et al.* nor Park, *et al.* teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Takahashi, *et al.* and Park, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claims 33, 36, and 38 are believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of claims 33, 36, and 38 under 35 U.S.C. 103(a) based on the combination of Takahashi, *et al.* and Park, *et al.* is respectfully requested.

With regard to the rejections of claims 10-12, 14-17, 23, 25, and 27-29 under 35 U.S.C. 103(a) based on the combination of Yamasaki, *et al.* and Sher, it is submitted that neither Yamasaki, *et al.* nor Sher teaches or suggests a semiconductor device comprising a control signal generating circuit receiving an input signal and generating a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from

the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in independent claims 10 and 23.

Yamasaki, *et al.* teaches a test mode setting circuit 3 that receives signals /RAS, /CAS, /WE, and Add (referred to in the Office Action as an input signal), and activates/deactivates a test mode designating signal TE (referred to in the Office Action as a control signal) when the signals are set to a predetermined combination of states (see Yamasaki, *et al.*, Figure 5A and page 7, paragraph [0092]). The Office Action at page 12, line 5 refers to the input signals, i.e., /RAS, /CAS, /WE, and Add, of Yamasaki, *et al.* controlling a TE control signal (see Yamasaki, *et al.*, Figure 5A), and further refers to signals /RAS, /CAS, /WE, and Add, of Yamasaki, *et al.* at Figure 5B as being simultaneously input, and affecting a change that is simultaneously output during a test period. However, there is no relationship between this asserted feature of Yamasaki, *et al.*, i.e., the input signals controlling a TE control signal, and the signals /RAS, /CAS, /WE, and Add being an input signal that is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in independent claims 10 and 23. Further, there is no relationship between this asserted feature of Yamasaki, *et al.* and the TE signal being a control signal that is activated when the signals /RAS, /CAS, /WE, and Add alone or in combination indicate that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, or the TE signal being a control signal that is inactivated when the signals /RAS, /CAS, /WE, and Add alone or in combination indicate that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is

less than the predetermined number of bits, as claimed in independent claims 10 and 23. In particular, there is no teaching or suggestion in Yamasaki, *et al.* of the signals /RAS, /CAS, /WE, and Add indicating that a number of data bits being simultaneously input to a semiconductor device or output from the semiconductor device is more or less than a predetermined number of bits, as claimed in claims 10 and 23.

The Office Action at page 12 further refers to the signals /RAS, /CAS, /WE, and Add controlling the number of data bits of the TE signal, which has more than one state, and a state can be considered a data bit. Applicants fail to understand this reasoning. One of skill in the art readily understands that a single bit has two states: off ('0') or on ('1'), 0 or 1, two bits have a total of four states, three bits have a total of eight states, etc. On the other hand, one of skill in the art would not agree that a state is considered a single data bit, as asserted in the Office Action.

Moreover, the issue of whether a state can be considered a data bit is not relevant to whether Yamasaki, *et al.* teaches that the signals /RAS, /CAS, /WE, and Add indicate that a number of data bits being simultaneously input to a semiconductor device or output from the semiconductor device is more or less than a predetermined number of bits, as claimed in claims 10 and 23. For example, even if each signal /RAS, /CAS, /WE, and Add of Yamasaki, *et al.* is simultaneously input to the test mode setting circuit 3, and assuming arguably that each signal /RAS, /CAS, /WE, and Add is one bit, there is nevertheless no comparison between the signals /RAS, /CAS, /WE, and Add and a predetermined number of bits.

Sher teaches a device that includes programmable circuits coupled to an external communication terminal such as a bond pad and to one of many load circuits such as input buffers, wherein the programmable circuits are configurable to load the terminal with one or more of the load circuits and to isolate the terminal from the rest of the load circuits (see Sher Summary of the Invention). The device of Sher includes an inventive IC die 10 comprising load

circuits 12 and 14 capable of communicating with external circuitry (not shown) through programmable circuits 16 and 18 and a terminal in the IC die 10, such as a bond pad 20 (see Sher, Figure 1). However, there is no teaching or suggestion in Sher of a semiconductor device comprising a control signal generating circuit receiving an input signal and generating a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 10 and 23.

In addition, it is submitted that Yamasaki, *et al.* and Sher fail to teach or suggest an internal voltage generating circuit coupled to the control signal generating circuit for receiving a control signal, as claimed in amended independent claims 10 and 23.

In particular, the Office Action at page 7 refers to Yamasaki, *et al.* as teaching an internal voltage generating circuit being coupled to the test mode setting circuit of Figure 5a of Yamasaki, *et al.* (referred to in the Office Action as a control signal generating circuit), and receiving a control signal TE. The test mode setting circuit of Figure 5a of Yamasaki, *et al.* outputs control signal TE to transfer gates 2c and 2e of driving circuit 2, and further outputs control signal TE to transistor 2f coupled to differential amplifier 2b (seeYamasaki, *et al.*, Figure 1). Thus, while the test mode setting circuit of Figure 5a of Yamasaki, *et al.* is coupled to various components of driving circuit 2, which generates a reference voltage Vrfo (see Yamasaki, *et al.,* Figure 1), there is no teaching or suggestion of the test mode setting circuit of

Figure 5a of Yamasaki, *et al.* being coupled to the voltage down converter VDC of Yamasaki, *et al.*, which generates an internal power supply voltage intVcc.

Sher teaches an integrated circuit die 10 that includes load circuits 12 and 14, circuits 16 and 18, and a terminal in the IC die 10, such as a bond pad 20 (see Sher, Figure 1). However, Sher likewise fails to teach or suggest an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, as claimed in amended independent claims 10 and 23.

Further, there is no teaching or suggestion in Yamasaki, *et al.* and Sher of an internal voltage generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim 23.

Yamasaki, *et al.* fails to teach or suggest that the abovementioned driving circuit 2 of Yamasaki, *et al.* is an internal voltage generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim 23. Specifically, there is no teaching or suggestion in Yamasaki, *et al.* of reference voltage Vrfo generated by driving circuit 2 being an internal voltage generated by an internal voltage generating circuit, as claimed in claim 10, or

making the internal voltage have the reference voltage level in response to a driving signal, as claimed in claim 23.

The Office Action at pages 12 and 13 refers to an internal voltage or external voltage being subjective relative to the circuit. The Office Action at page 13 further refers to the voltage being transmitted to a pad in Yamasaki, *et al.* being internal to the circuit of Yamasaki, *et al.* However, the Office Action at page 9 refers to voltage intVcc as being an internal voltage, and that the voltage transmitted to the pad, i.e., Vrfo, is a reference voltage that is compared to the voltage intVcc. Applicants therefore submit that, regardless of whether voltage Vrfo is internal to the circuit of Yamasaki, *et al.*, voltage Vrfo is different than the internal voltage intVcc of Yamasaki, *et al.*, and therefore, there is no teaching or suggestion in Yamasaki, *et al.* of reference voltage Vrfo generated by driving circuit 2 being an internal voltage generated by an internal voltage generating circuit, as claimed in claim 10, or making the internal voltage have the reference voltage level in response to a driving signal, as claimed in claim 23.

Further, there is no teaching or suggestion in Yamasaki, *et al.* of voltage intVcc being an internal voltage generated by an internal voltage generating circuit, as claimed in claim 10, or making the internal voltage have the reference voltage level in response to a driving signal, as claimed in claim 23. Thus, it follows that neither the comparator CMP nor the amplifying circuit 2b of the driving circuit 2 of Yamasaki, *et al.* is a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim 23.

With regard to Sher, there is no teaching or suggestion in Sher of an internal voltage

generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim 23.

The Office Action at page 13 asserts that Applicants provide arguments against the references individually. Applicants respectfully submit that they are not engaging in a piecemeal analysis herein. Instead, Applicants' arguments are directed to the combination of the references. That is, since neither Yamasaki, *et al.* nor Sher, taken alone, teaches or suggests the elements of the present invention identified herein, as claimed in claims 10 and 23, there is no combination of Yamasaki, *et al.* and Sher that would provide such teaching or suggestion.

Applicants therefore respectfully submit that, instead of being a piecemeal analysis of the references individually, the foregoing is directed to the cited combination of references, notwithstanding the necessity to discuss the contents of each of the Yamasaki, *et al.* and Sher references.

Accordingly, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest the invention set forth in amended independent claims 10 and 23. Specifically, neither Yamasaki, *et al.* nor Sher teaches or suggests a semiconductor device comprising a control signal generating circuit receiving an input signal and generating a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input

to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 10 and 23, or an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, as claimed in amended independent claims 10 and 23, or an internal voltage generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim 23.

Since neither Yamasaki, *et al.* nor Sher teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since the combination of Yamasaki, *et al.* and Sher fails to teach or suggest the invention set forth in the claims, the claims are believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection of claims 10-12, 14-17, 23, 25, and 27-29 under 35 U.S.C. 103(a) based on the combination of Yamasaki, *et al.* and Sher are respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Authorization is hereby given to charge Deposit Account No. 501798 for any fees which may be due or to credit any overpayment.

Respectfully submitted,

Steven M. Mills
Registration Number 36,610
Attorney for Applicants

Date: 9/26/08

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0529\073108 OA\amendmenth_afterfinal.doc